W-BAND MMIC VCO WITH A LARGE TUNING RANGE USING A PSEUDOMORPHIC HFET

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ABSTRACT

A widely tunable oscillator with a center frequency of 94 GHz including a two stage buffer amplifier has been designed and fabricated. The output power was 6 mW. The mechanical tuning range by removing airbridges was 18 GHz. The electrical tuning range was 8 GHz. The noise performance was better than -67 dBc/Hz at 1 MHz from the carrier.

INTRODUCTION

MMICs for systems operating in the W-band are of growing interest for many applications, e.g. for FMCW radar systems [1]. For such systems, the millimeter wave source has a major key position.

Monolithic integrated W-band oscillators utilizing FETs as active devices are under investigation since many years. In 1985, Tserng et al. [2] built a 100 GHz GaAs FET oscillator with an output power of 0.1 mW and a tuning range of 250 MHz. An acceptable output power of 14 mW and a good phase noise behavior of -70 dBc/Hz at 15 kHz offset to a carrier frequency of 92 GHz was reported by Schellenberg et al. [3] by using an InGaAs MESFET with an recangular waveguide as resonator element. Four years ago, Wang et al. [4] presented a monolithic W-band VCO using pseudomorphic HEMTs. The output power was approximately 8 mW at 90 GHz. The tuning range was 600 MHz. The phase noise was about 68 dBc/Hz for an offset frequency of 1 MHz. Using InP-based HEMTs, Kwon et al. [5] reported a 130 GHz oscillator with an output power of 0.15 mW. The tuning range was 400 MHz wide.

In this work, we present the design, fabrication and performance of a MMIC VCO using pseudomorphic HFETs. The oscillator is widely tunable. The output power is 6 mW.

STRUCTURE OF ACTIVE DEVICE

The layers for the HFETs were grown on s.i. 3" GaAs wafers by MBE. The vertical structure is as follows: GaAs buffer including an AlGaAs/GaAs superlattice, 12 nm $In_{0.25}Ga_{0.75}As$ channel, 5 nm $Al_{0.2}Ga_{0.8}As$ spacer, 20 nm $Al_{0.2}Ga_{0.8}As$ supply layer including n-type δ-doping in a thin GaAs layer, 3 nm n-GaAs etch stop, 3 nm $Al_{0.2}Ga_{0.8}$ As etch stop, and 30 nm n^+-GaAs cap layer.

The lateral structure of the device was realized by a dry etching process for the recessed gates in combination with alloyed drain and source electrodes. The Ti/Pt/Au gate metallization is placed in the recess onto the n-GaAs etch stop layer. The gate length is 0.15 µm and the gate width of the HFETs is 2x20 µm. The drain and source electrodes were evaporated on the n^+-GaAs cap layer. These ohmic contacts were alloyed into the buffer layer above the superlattice. The source to drain spacing is 1.1 µm.

OSCILLATOR CIRCUIT

For the oscillator circuit, a simple T-type configuration, (Fig. 1) was chosen, with coplanar lines as resonator elements. The non-linear simulation was performed using the HP-EEsof

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software LIBRA. The active device was measured and characterized over the frequency range of 0.5-75 GHz. The transistor model was implemented in the simulation tool using the EEHEMT model.

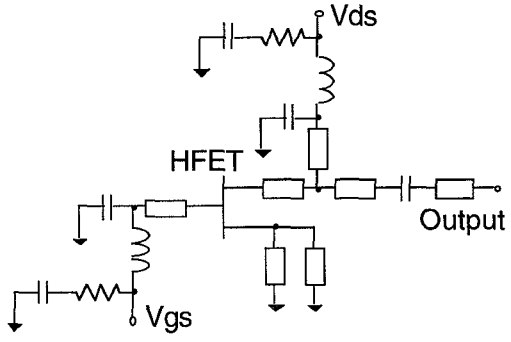

Fig. 1: Schematic circuit diagram of the oscillator.

The gate terminal is connected to a MIM capacitor (C = 3 pF) by a coplanar line (CPL) with 70 Ω characteristic impedance and a length of l_{lg}=70 µm. The other side of the integrated MIM capacitor is connected to ground, allowing the supply of a gate bias voltage. Due to the geometry of the HFET, the source is grounded through two symmetric CPLs. The length of these lines is variable between a length of l_{lsmin}=200 µm to l_{lsmax}=400 µm in steps of 50 µm. The drain bias is supplied by a CPL shorted stub of length of l_{ld}=310 µm which is also part of the output matching network of the oscillator. The realized MMIC, which has a chip size of only 2.5x1 mm^2, is depicted in Fig. 2. The oscillator stage can be seen in the right hand side of the photograph.

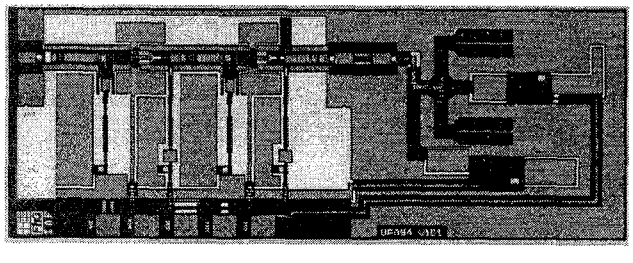

Fig. 2: Microphotograph of the realized oscillator (chip size: 2.5x1 mm^2).

The effective length of the source resonator lines was adjustable by removing a set of airbridges. Fig. 3 shows a microphotograph of one of the resonator lines before and after mechanical tuning. The CPL has a characteristic impedance of 70 Ω. The ground-to-ground spacing is tapered from d_1=50 µm to d_2=100 µm. This easily allows a coarse tuning of the oscillation frequency. Fine tuning could be achieved by varying the gate voltage of the oscillator FET.

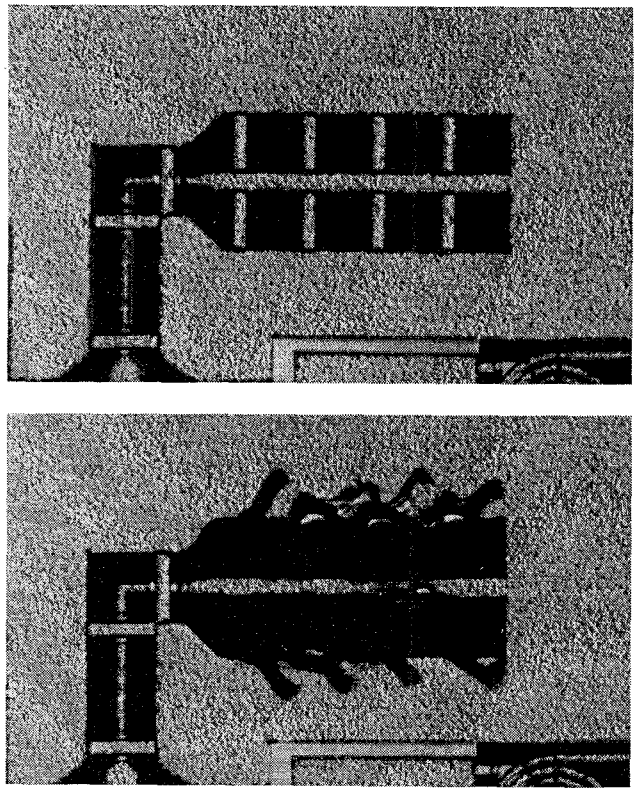

Fig. 3: CPW-resonator before and after mechanical tuning by removing airbridges.

AMPLIFIER CIRCUIT

The amplifier circuit is a two stage reactively matched design using cascode type FETs of a gate width of 2x40 µm, each. Design and layout of the circuit is based on a work published earlier [5]. The schematic diagram is depicted in Fig. 4. The devices have a f_T and f_{max} of 120 GHz and 200 GHz, respectively. We have recently utilized cascode FETs for integrated reactive matched amplifiers because of their higher gain and thus lower chip size requirement as compared to conventional single gate FETs. A two stage W-band amplifier was designed to cover the 90-100 GHz frequency range. Coplanar lines

with 50 Ω characteristic impedance were used to construct the reactive matching networks. For the amplifier design, a scalable cascode FET model was used based on single FET models at the relevant bias points. The gain of the amplifier is 25ÊdB at 94 GHz.

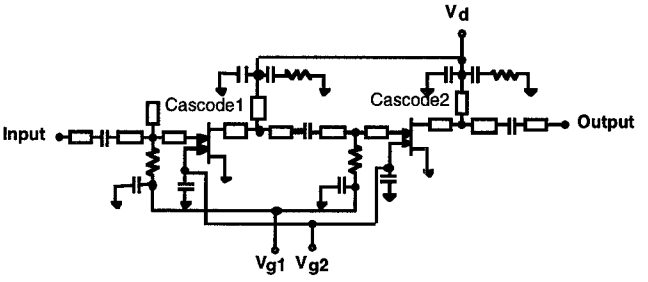

Fig. 4: Schematic diagram of the two stage amplifier circuit.

EXPERIMENTAL SETUP

The oscillator was characterized on-wafer. To ensure high-quality supply voltages a semiconductor parameter analyzer was used as power supply, delivering four different voltages for the operation of the oscillator: the oscillator tuning voltage V_{gs}, the drain voltage for both, the oscillator and the amplifier stage, V_{ds}, and the two control voltages for the gates of the cascode FETs, V_{g1} and V_{g2}, respectively. The output power was measured by a power meter in combination with a W-band power sensor. The spectrum of the oscillator signal was monitored on a spectrum analyzer using a harmonic mixer in combination with a 10 dB coupler and a 10 dB attenuator.

EXPERIMENTAL RESULTS

First, we examined the tuning behavior of the oscillator. The frequency of oscillation was varied by altering the tuning voltage. After measurement of each curve, two pairs of airbridges (one pair for each resonator) were removed. Hence, the effective length of the resonating elements was varied in steps of 50 µm.

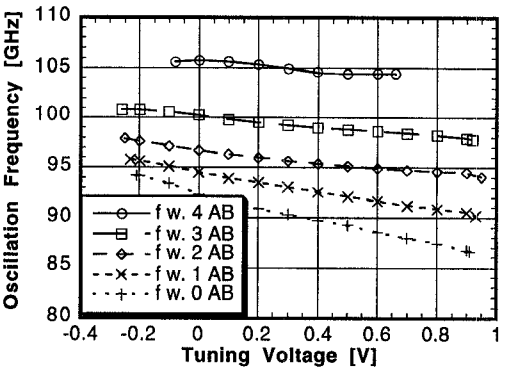

Fig. 5: Oscillation frequency vs. tuning voltage with different number of airbridges.

The diagram in Fig. 5 shows the oscillation frequency in dependence on the tuning voltage V_{gs}. The coarse adjustment covers the frequency range between 87 GHz and 105 GHz (except 101 GHz to 104 GHz). The slope of the curves varies with the effective length of the resonators between 4 GHz/V and 7 GHz/V. The fine adjustment by electrical tuning covers at maximum (with all airbridges removed) a frequency range of approximately 8 GHz. There are wide ranges of a nearly linear relation between the frequency and the tuning voltage.

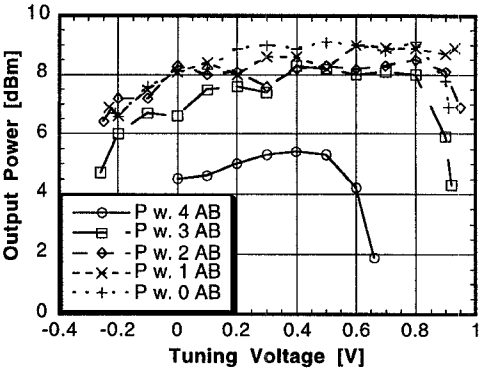

Fig. 6: Measured output power vs. tuning voltage.

At the same time, we measured the output power at the different frequencies. As shown in Fig. 6, the output power was approximately P_{out}=8 dBm over a wide frequency range. Due to

the frequency response of the amplifier and the oscillator circuit, the output power in the highest frequency range (with all 4 airbridges) decreases to about P_{out}=5 dBm. In all other configurations the output power is nearly constant.

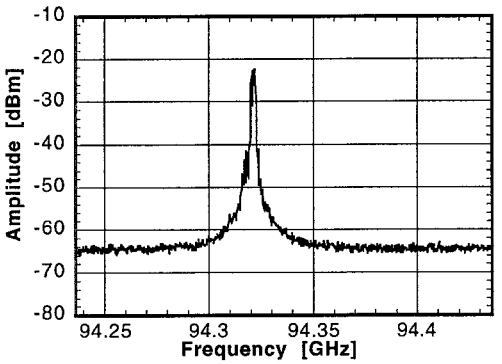

Fig. 7: Output spectrum of the oscillator.

The output spectrum of the oscillator is depicted in Fig. 7. It was measured in a configuration with two airbridges. The phase noise behavior in a distance of 10 MHz from the carrier was measured and subsequently converted to the noise in a 1 MHz offset by adding 30 dB. This leads to a typical phase noise performance of better than -67 dBc/Hz at 1 MHz offset from the carrier.

CONCLUSION

A W-band MMIC oscillator including a two stage buffer amplifier was designed and fabricated with our in-house technology. The experimental results show an output power of 6 mW at an oscillation frequency of 94 GHz. The large tuning range combined with an acceptable noise behavior, which can be further improved, makes it suitable for many system applications.

ACKNOWLEDGEMENT

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